SIMPLE RISC-LIKE ARCHITECTURE

SIMPLE MICROPROCESSOR

WITH LIMITED INSTRUCTIONS

ADIPTA HALDER

21EC30003

IIT KHARAGPUR

GENERAL INFORMATION ABOUT THE MICROPROCESSOR

**CLOCK TIME PERIOD = 6 ns**

**HARDWIRED CONTROL UNIT**

**32 BITS INSTRUCTION**

**16 BITS DATA**

GENERAL PURPOSE REGISTERS

**14 GENERAL PURPOSE 16 BIT REGISTERS**

**ACCUMULATOR**

**DATA REGISTER**

SPECIAL PURPOSE REGISTERS

**PROGRAM COUNTER (16 BITS)**

**DATA MEMORY ADDRESS REGISTER (16 BITS)**

**INSTRUCTION MEMORY ADDRESS REGISTER (16 BITS)**

**MEMORY DATA REGISTER (16 BITS)**

**INSTRUCTION REGISTER (32 BITS)**

ALU MODULE

**ADDER**

**SUBTRACTOR**

**LOGICAL AND**

**LOGICAL OR**

**LOGICAL XOR**

**LOGICAL NOT**

**MEMORY MODULES**

DATA MEMORY (35536 X 16): 16 BIT ADDRESS (2^16 MEMORY LOCATIONS 16 BIT EACH)

INSTRUCTION MEMORY (35536 X 32): 16 BIT ADDRESS (2^16 MEMORY LOCATIONS 32 BIT EACH)

ADDRESSING MODES

1. REGISTER ADDRESSING (ALL OPERANDS ARE REGISTERS)
2. IMMEDIATE ADDRESSING (ONLY 1 IMMEDIATE ALLOWED)
3. BASE OFFSET ADDRESSING
4. DIRECT ADDRESSING
5. INDIRECT ADDRESSING
6. PC RELATIVE ADDRESSING (FOR BRANCHING)

ISA AND DETAILS OF OPERATION

ARITHMETIC LOGIC INSTRUCTIONS

**ADDRESSING MODE 1: BASIC ALU OPERATIONS BETWEEN 2 REGISTERS & STORE IN A REG (CLASS 1)**

**LIST OF OPERATIONS:**

* 0000 0000 = ADD WITH CARRY
* 0000 0100 = SUB WITH CARRY 0001 0000 = BITWISE AND
* 0001 0100 = BITWISE XOR
* 0001 1000 = BITWISE OR
* 0001 1100 = BITWISE NOT

**INSTRUCTION DETAILS:**

* IR [3:0] --> SOURCE REG 1
* IR [7:4] --> SOURCE REG 2
* IR [11:8] --> DEST REG

**ADDRESSING MODE 2: BASIC ALU OPS BETWEEN A REG AND AN IMMEDIATE & STORE IN A REG (CLASS 2)**

**LIST OF OPERATIONS:**

0000 0001 = ADD WITH CARRY **(CARRY STORED IN CARRY FLAG)**

0000 0101 = SUB WITH CARRY **(CARRY DENOTED IN CARRY FLAG AND OVERFLOW DENOTED IN OVERFLOW FLAG)**

0001 0001 = BITWISE AND

0001 0101 = BITWISE XOR

0001 1001 = BITWISE OR

0001 1101 = BITWISE NOT

**INSTRUCTION DETAILS:**

* IR [3:0] --> SOURCE REG 1
* IR [7:4] --> DEST REG
* IR [23:8] --> IMMEDIATE VALUE

**REGISTER TRANSFER AND IMMEDIATE LOADING**

**ADDRESSING MODE 2: IMMEDIATE DATA LOAD INTO A REG (CLASS 4)**

**OPCODE LIST:**

* 0010 0001

**INSTRUCTION DETAILS:**

* IR [3:0] --> DEST REG
* IR [8:23] --> IMMEDIATE VALUE

**ADDRESSING MODE 1: TRANSFER BETWEEN 2 REGISTERS (CLASS 5)**

**OPCODES LIST:**

* 0010 0000

**INSTRUCTION DETAILS:**

* IR [3:0] --> SRC REG
* IR [7:4] --> DEST REG

**MEMORY LOAD & STORE**

**ADDRESSING MODE 4: STORE SOME DATA FROM ANY REG DIRECTLY TO ANY MEMORY LOCATION (CLASS 6)**

**OPCODE LIST:**

01000000

**INSTRUCTION DETAILS:**

* IR [3:0] --> SRC REG
* IR [8:23] --> ADDRESS IN DATA MEMORY

**ADDRESSING MODE 4: LOAD SOME DATA DIRECTLY FROM ANY MEMORY LOCATION TO ANY REG (CLASS 7)**

**OPCODE LIST:**

01001000

**INSTRUCTION DETAILS:**

* IR [3:0] --> SRC REG
* IR [8:23] --> ADDRESS IN DATA MEMORY

**ADDRESSING MODE 5: STORE SOME DATA FROM ANY REG DIRECTLY TO ANY MEMORY LOCATION OBTAINED FROM ANOTHER REG (CLASS 8)**

**OPCODE LIST:**

0101 0000

**INSTRUCTION DETAILS:**

* IR [3:0] --> SRC REG
* IR [7:4] --> ADDRESS REG

**ADDRESSING MODE 5: LOAD SOME DATA FROM ANY MEMORY LOCATION TO ANY REG (CLASS 9)**

**OPCODE LIST:**

0101 1000

**INSTRUCTION DETAILS:**

* IR [3:0] --> SRC REG
* IR [7:4] --> ADDRESS REG

**ADDRESSING MODE 3: STORE SOME DATA FROM ANY REG USING BASE OFFSET TO ANY MEMORY LOCATION (CLASS 10)**

**OPCODE LIST:**

0101 1001

**INSTRUCTION DETAILS:**

* IR [3:0] --> SRC REG
* IR [7:4] --> BASE REG
* IR [23:8] --> OFFSET

**ADDRESSING MODE 3: LOAD SOME DATA FROM ANY MEMORY LOCATION USING BASE OFFSET TO ANY REG (CLASS 11)**

**OPCODE LIST:**

0101 1010

**INSTRUCTION DETAILS:**

* IR [3:0] --> DEST REG
* IR [7:4] --> BASE REG
* IR [23:8] --> OFFSET

**BRANCH INSTRUCTIONS**

**ADDRESSING MODE 6: UNCONDITIONAL BRANCH (CLASS 12)**

**OPCODES LIST:**

01100000

**INSTRUCTION DETAILS:**

* IR [23:8] --> OFFSET

**ADDRESSING MODE 6: JUMP/ BRANCH IF REGISTER A =B (CLASS 13)**

**OPCODES LIST:**

01100001

**INSTRUCTION DETAILS:**

* IR [3:0] --> SRC REG 1
* IR [7:4] --> SRC REG 2
* IR [15:0] --> OFFSET

**ADDRESSING MODE 6: JUMP/ BRANCH IF REGISTER A < B (CLASS 14)**

**OPCODES LIST:**

01100010

**INSTRUCTION DETAILS:**

* IR [3:0] --> SRC REG 1
* IR [7:4] --> SRC REG 2
* IR [15:0] --> OFFSET

**ADDRESSING MODE 6: JUMP/ BRANCH IF REGISTER A > B (CLASS 15)**

**OPCODES LIST:**

01100011

**INSTRUCTION DETAILS:**

* IR [3:0] --> SRC REG 1
* IR [7:4] --> SRC REG 2
* IR [15:0] --> OFFSET